VIMAL JYOTHI ENGINEERING COLLEGE
CHEMPERI KANNUR.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

S3-ECL203 LOGIC DESIGN LAB

Sl. No.	LIST OF EXPERIMENTS
1	Realization of functions using basic and universal gates (SOP and POS forms).
2	Design and Realization of half /full adder and subtractor using basic gates and universal gates.
3	Adder / Subtractor Circuits Using 7483
4	Study of Flip Flops: S-R, D, T, JK and Master Slave JK FF using NAND gates
5	Asynchronous Counter:3 bit up/down counter
6	Synchronous Counter: Realization of 4-bit up/down counter
7	Ring Counter and Johnson Counter
8	Realization of Logic Gates and Familiarization of verilog
9	Adders in Verilog
10	Mux and Demux in Verilog
11	Flipflops and counters in Verilog