CONTINUOUS INTERNAL ASSESSMENT - LAB

- **Evaluation of the Practical course: Lab involvement, Records, Written test**

TOTAL MARKS	CIE	ESE	ESE DURATION
150	75	75	3 HOURS

Continuous *internal Evaluation Pattern*

Attendance : 15 marks
Continuous Assessment : 30 marks
Internal Test : 30 marks

- For continuous assessment marks are given for

1. Implementation
2. Record
3. Viva

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ECL 203	LOGIC DESIGN LAB	CATEGORY	L	T	P	CREDIT
		PCC	0	0	3	2

Preamble: This course aims to (i) familiarize students with the Digital Logic Design through the implementation of Logic Circuits using ICs of basic logic gates (ii) familiarize students with the HDL based Digital Design Flow.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Design and demonstrate the functioning of various combinational and sequential circuits using ICs
CO 2	Apply an industry compatible hardware description language to implement digital circuits
CO 3	Implement digital circuis on FPGA boards and connect external hardware to the boards
CO 4	Function effectively as an individual and in a team to accomplish the given task

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3	3						3			3
CO 2	3	1	1	3	3				3			3
CO 3	3	1	1	3	3				3	1		3
CO 4	3	3	3		3				3			3

Assessment

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	75	75	2.5 hours

Continuous Internal Evaluation Pattern:

Attendance : 15 marks
Continuous Assessment : 30 marks

ELECTRONICS AND COMMUNICATION ENGINEERIN

Internal Test (Immediately before the second series test) : 30 marks

End Semester Examination Pattern: The following guidelines should be followed regarding award of marks

(a) Preliminary work : 15 Marks
(b) Implementing the work/Conducting the experiment : 10 Marks
(c) Performance, result and inference (usage of equipments and trouble shooting) : 25 Marks
(d) Viva voce : 20 marks
(e) Record : 5 Marks

General instructions: End-semester practical examination is to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

Course Level Assessment Questions

Course Outcome 1 (CO1): Design and Development of combinational circuits

1. Design a one bit full adder using gates and implement and test it on board.
2. Implement and test the logic function f(A,B,C)=∑m(0,1,3,6) using an 8:1 Mux IC
3. Convert a D flip-flop to T flip-flop and implement and test on board.

Course Outcome 2 and 3 (CO2 and CO3): Implementation of logic circuits on tiny FPGA

1. Design and implement a one bit subtracter in Verilog and implement and test it on a tiny FPGA board.
2. Design and implement a J-K flip-flop in Verilog, implement and test it on a tiny FPGA board.
3. Design a 4:1 Multiplexer in Verilog and implement and test it on tiny FPGA board.

List of Experiments:

It is compulsory to conduct a minimum of 5 experiments from Part A and a minimum of 5 experiments from Part B.

Part A (Any 5)

The following experiements can be conducted on breadboard or trainer kits.

1. Realization of functions using basic and universal gates (SOP and POS forms).
2. Design and Realization of half /full adder and subtractor using basic gates and universal gates.
3. 4 bit adder/subtractor and BCD adder using 7483.
4. Study of Flip Flops: S-R, D, T, JK and Master Slave JK FF using NAND gates.
5. Asynchronous Counter:3 bit up/down counter

Sample Syllabus- Lab

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Vimal Jyothi Engineering College

Department of Electronics Communication and Engineering (EC)

Daily Lab Score

USN	Name	Exp 1	Exp 2	Exp 3	Exp 4	Exp 5	Exp 6	Exp 7	Exp 8	Exp 9	Exp 10	Aggregate
LVML21EC052	Sidharth C	25	25	28	30	29	25	25	29	29	29	28
LVML21EC053	Vishnupriya M P	25	25	30	29	29	30	30	30	30	30	29
SCT21EC088	Samved Vivek	0	0	0	0	0	0	0	0	0	0	0
VML21EC028	Ivin Joseph R ajesh	25	22	25	24	23	30	30	30	30	30	27
VML21EC029	Jesna Maria	23	22	24	27	27	29	30	29	30	30	28
VML21EC030	Jessay Jose A ntony	23	22	30	30	30	28	29	30	30	29	29
VML21EC031	Jestel Joseph	30	23	26	24	23	30	28	28	30	28	27
VML21EC032	Jibin Varghe se	28	28	25	30	20	0	0	0	20	20	18
VML21EC033	Jishnu Prakas h K K	25	25	30	28	28	30	30	30	27	30	29
VML21EC034	K Amith Babu	28	30	28	29	28	30	30	30	30	30	30
VML21EC035	Manu Roy	25	22	30	27	28	30	29	30	29	29	28
VML21EC036	Martin Reju	29	29	28	30	30	30	30	30	30	30	30
VML21EC037	Midhun Mad hav M	25	22	30	29	29	30	25	28	30	30	28
VML21EC038	Muhammad S aleeth	25	30	25	29	30	30	30	30	30	30	29
VML21EC039	Muhammed A adil Ashraf	25	25	29	28	28	24	25	28	28	29	27
VML21EC040	Navya.t	30	25	25	29	27	30	25	29	30	30	28
VML21EC041	Neha.m	25	22	29	29	29	29	30	29	30	30	29
VML21EC042	Rana Noufal	29	28	25	30	28	30	28	30	30	30	29
VML21EC043	Ridwik M R	28	26	30	24	30	30	30	30	30	30	29
VML21EC044	Sayand Shin e K	25	25	24	30	28	30	28	30	30	30	28
VML21EC045	Sebastian Jos eph	29	25	30	28	28	30	29	29	30	30	29
VML21EC046	Soorya M S	28	24	29	30	30	30	27	30	30	30	29
VML21EC047	Sreelal P V	28	29	30	29	30	30	30	30	30	30	30
VML21EC048	Theertha Sunil	25	25	23	22	28	29	28	28	30	30	27
VML21EC049	Vaishnavi E	30	29	28	30	30	30	27	29	29	30	30
VML21EC050	Vishakh Sasi	30	29	30	30	28	30	30	30	30	30	30
VML21EC051	Vismaya C	30	27	25	29	29	30	30	30	30	30	29

Sample copy of daily lab score

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INDEX

Exp. No.	Date	Name of the Experiment	Page No.	Marks	Signature of the Faculty
1.	9/2/23	Arithmetic operations using 8051	14-19	25	
2.	16/2/23	Sum of a series of 8 bit using 8051	21-23	15	
3.	16/3/23	Data Transfer operation using 8051	24-27	28	
4.	16/3/23	Largest element in an Array using 8051	28-31	30	
5.	23/3/23	Square of a Number	32-35	30	
6.	23/3/23	Square root of a Number	36-39	30	
7.	30/3/23	Hexadecimal to decimal conversion	40-43	30	
8.	4/4/23	Stepper Motor Interfacing with 8051	44-51	30	
9.	13/4/23	ADC Interfacing with 8051	52-57	30	
10.	13/4/23	DAC Interfacing with 8051	58-63	30	
11	1/6/23	Decimal to Hexadecimal conversion	64-67	30	
12.	1/6/23	Smallest element in an array using 8051.	68-71	30	
		Completed 12 Experiments			
		26/6/23			

Sample copy of lab record front page

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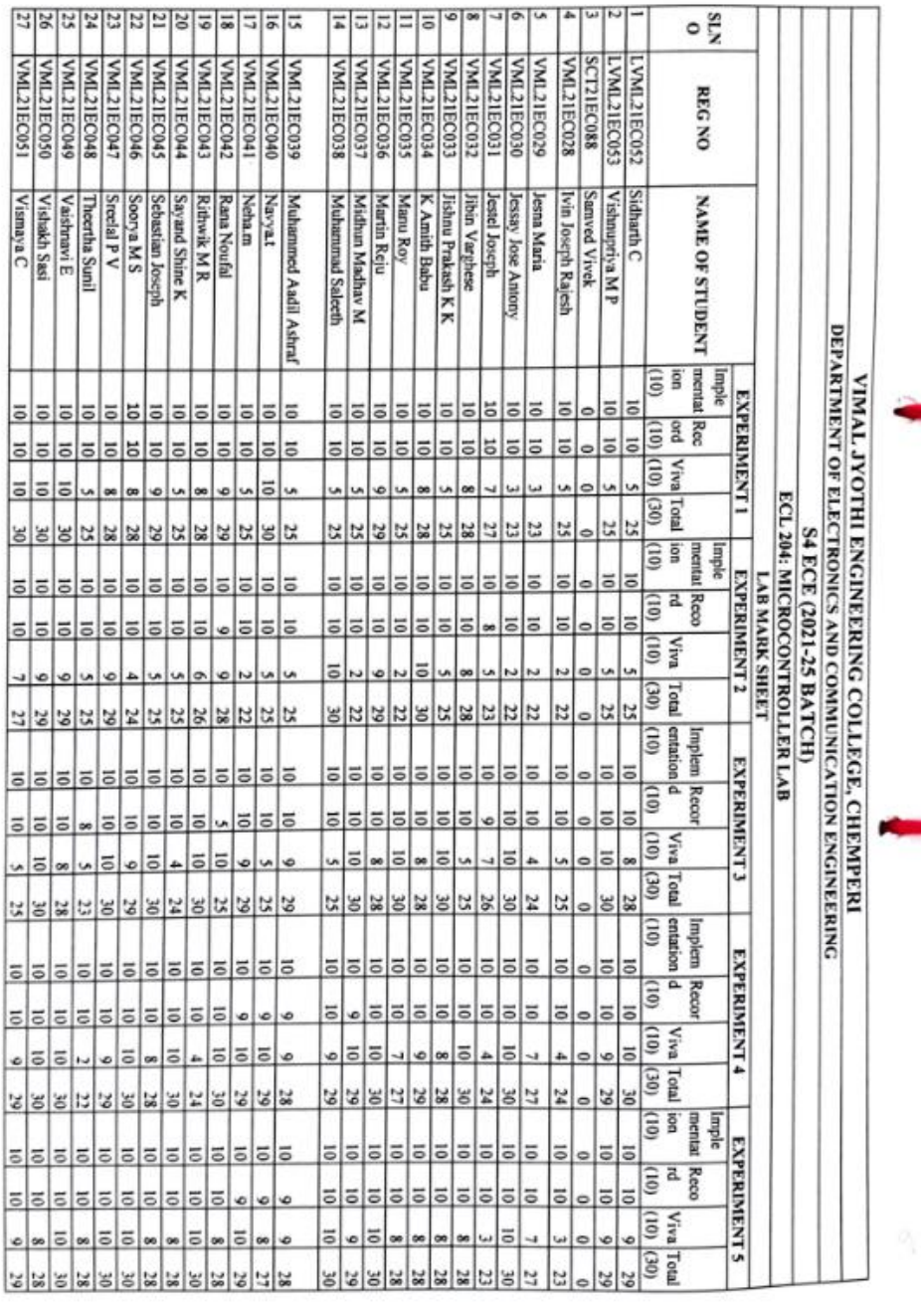

VIMAL JYOTHI ENGINEERING COLLEGE, CHEMPERI
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
S4 ECE (2021-25 BATCH)
ECL 204: MICROCONTROLLER LAB
LAB MARK SHEET

SLNO	REG NO	NAME OF STUDENT	EXPERIMENT 1					EXPERIMENT 2					EXPERIMENT 3					EXPERIMENT 4					EXPERIMENT 5				
			Implementation (10)	Record (10)	Viva (10)	Total (30)	Implementation (10)	Record (10)	Viva (10)	Total (30)	Implementation (10)	Record (10)	Viva (10)	Total (30)	Implementation (10)	Record (10)	Viva (10)	Total (30)	Implementation (10)	Record (10)	Viva (10)	Total (30)	Implementation (10)	Record (10)	Viva (10)	Total (30)
1	LVML21EC052	Sidharth C	10	10	5	25	10	10	5	25	10	10	8	28	10	10	9	29	10	10	9	29	10	9	9	28
2	LVML21EC053	Vishnupriya M P	10	10	5	25	10	10	5	25	10	10	10	30	10	10	9	29	10	10	9	29	10	10	9	28
3	SCT21EC088	Samved Vivek	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	VML21EC028	Irin Joseph Rajesh	10	10	5	25	10	10	2	22	10	10	5	25	10	10	4	24	10	10	4	24	10	10	3	23
5	VML21EC029	Jesna Maria	10	10	3	23	10	10	2	22	10	10	4	24	10	10	7	27	10	10	7	27	10	10	7	27
6	VML21EC030	Jessy Jose Antony	10	10	3	23	10	10	2	22	10	10	10	30	10	10	10	30	10	10	10	30	10	10	10	30
7	VML21EC031	Jestel Joseph	10	10	7	27	10	8	5	23	10	9	7	26	10	10	4	24	10	10	4	24	10	10	3	23
8	VML21EC032	Jibin Varghese	10	10	8	28	10	10	8	28	10	10	5	25	10	10	10	30	10	10	8	28	10	10	8	28
9	VML21EC033	Jishnu Prakash K K	10	10	5	25	10	10	5	25	10	10	10	30	10	10	8	28	10	10	9	29	10	10	8	28
10	VML21EC034	K. Amith Babu	10	10	8	28	10	10	10	30	10	10	8	28	10	10	9	29	10	10	7	27	10	10	8	28
11	VML21EC035	Manu Roy	10	10	5	25	10	10	2	22	10	10	10	30	10	10	7	27	10	10	8	28	10	10	8	28
12	VML21EC036	Martin Reju	10	10	9	29	10	10	9	29	10	10	8	28	10	10	7	27	10	10	10	30	10	10	10	30
13	VML21EC037	Midhun Madhav M	10	10	5	25	10	10	2	22	10	10	10	30	10	10	9	29	10	10	10	30	10	10	9	29
14	VML21EC038	Muhammad Saleeth	10	10	5	25	10	10	10	30	10	10	5	25	10	10	10	30	10	10	9	29	10	10	10	30
15	VML21EC039	Muhammed Aadil Ashraf	10	10	5	25	10	10	5	25	10	10	9	29	10	9	9	28	10	9	9	28	10	9	9	28
16	VML21EC040	Navya.t	10	10	10	30	10	10	5	25	10	10	5	25	10	10	9	29	10	10	10	30	10	10	8	27
17	VML21EC041	Neha.m	10	10	5	25	10	10	2	22	10	10	9	29	10	10	10	30	10	9	10	29	10	9	10	29
18	VML21EC042	Rana Noufal	10	10	9	29	10	9	9	28	10	5	10	25	10	10	10	30	10	10	10	30	10	10	8	28
19	VML21EC043	Ribwik M R	10	10	8	28	10	10	6	26	10	10	10	30	10	10	4	24	10	10	4	24	10	10	10	30
20	VML21EC044	Sayand Shine K	10	10	5	25	10	10	5	25	10	10	4	24	10	10	10	30	10	10	10	30	10	10	8	28
21	VML21EC045	Sebastian Joseph	10	10	9	29	10	10	5	25	10	10	10	30	10	10	8	28	10	10	10	30	10	10	8	28
22	VML21EC046	Soorya M S	10	10	8	28	10	10	4	24	10	10	9	29	10	10	10	30	10	10	8	28	10	10	8	28
23	VML21EC047	Sreelal P V	10	10	8	28	10	10	9	29	10	10	10	30	10	10	9	29	10	10	9	29	10	10	10	30
24	VML21EC048	Theertha Sunil	10	10	5	25	10	10	5	25	10	8	5	23	10	10	2	22	10	10	8	28	10	10	8	28
25	VML21EC049	Vaishnavi E	10	10	10	30	10	10	9	29	10	10	8	28	10	10	10	30	10	10	10	30	10	10	10	30
26	VML21EC050	Vishakh Sasi	10	10	10	30	10	10	9	29	10	10	10	30	10	10	10	30	10	10	10	30	10	10	8	28
27	VML21EC051	Vismaya C	10	10	10	30	10	10	7	27	10	10	5	25	10	10	9	29	10	10	9	29	10	10	9	29

Vidhisana Vijayan 24/10/23

Continuous evaluation mark -lab

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Vimal Jyothi Engineering College
Office Order

VJEC/ECE/EXE/2023

Sub:IV Sem. B.Tech Degree Practical Examination June 2023–Conductof Internal Practical Examination

Practical of IV Sem. B.Tech Degree (2021-2025 Batches)is scheduled to be held on 26/06/23 Monday and 27/06/23 Tuesday as per the following schedule.

SL No	Course	Date	Time	Roll Numbers	Examiners
1	ECL202 ANALOG CIRCUITS AND SIMULATION LAB	26.6.23	9:00-11:30	VML21EC028-VML21EC041	Examiner: Mr. Vinod J Thomas and Mr.Manoj K C
			10:30 -1:00	VML21EC042-VML21EC051, LVML21EC052, LVML21EC053, SCT21EC088	
		27.6.23	9:00-11:30	VML21EC001-VML21EC014	
			10:30 -1:00	VML21EC015-VML21EC027	

SL No	Course	Date	Time	Roll Numbers	Examiners
1	ECL204 MICROCONTROLLER LAB	26.6.23	9:00-11:30 AM	VML21EC001-VML21EC014	Examiner: Ms Anusha Chacko and Ms Sudharsana Vijayan
			10:30AM - 01:00PM	VML21EC015-VML21EC027	
		27.6.23	9:00-11:30 AM	VML21EC028-VML21EC041	
			10:30AM - 01:00PM	VML21EC042-VML21EC051 LVML21EC052,LVML21EC053, SCT21EC088	

24/6/23
Sudharsana Vijayan
LAB IN CHARGE

HODECE

Lab internal exam -office order

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VIMAL JYOTHI ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ECL 204-MICROCONTROLLER LAB

SEMESTER 4 (2021-25 BATCH)

Date Of Exam Conducted: 26th to 27th June 2023

SLNO	USN / Candidate ID	NAME OF STUDENTS	DATE & TIME	SIGNATURE
1	VML21EC001	Abhinav Prakash	26.06.23 9.00 AM	
2	VML21EC002	Abhinav Sujith	26.06.23 9.00 AM	
3	VML21EC003	Adarsh K B	26.06.23 9.00 AM	
4	VML21EC004	Aeibel Tomy	26.06.23 9.00 AM	
5	VML21EC005	Ahammed Sinan Muhammed	26.06.23 9.00 AM	
6	VML21EC006	Ajaynath P	26.06.23 9.00 AM	
7	VML21EC007	Akarsh Kc	26.06.23 9.00 AM	
8	VML21EC008	Alanta George	26.06.23 9.00 AM	
9	VML21EC009	Amal Sony	26.06.23 9.00 AM	
10	VML21EC010	Amith Vinesh	26.06.23 9.00 AM	
11	VML21EC011	Amrutha A Nair	26.06.23 9.00 AM	
12	VML21EC012	Ananya K	26.06.23 9.00 AM	
13	VML21EC013	Angel Mary	26.06.23 9.00 AM	
14	VML21EC014	Ann Mariya Chacko	26.06.23 9.00 AM	
15	VML21EC015	Anold Tomy	26.06.23 10.30 AM	
16	VML21EC016	Anukrishna P V	26.06.23 10.30 AM	
17	VML21EC017	Arya Alakkandy	26.06.23 10.30 AM	
18	VML21EC018	Aswin P	26.06.23 10.30 AM	
19	VML21EC019	Belfin Baby	26.06.23 10.30 AM	
20	VML21EC020	Ben Augustine	26.06.23 10.30 AM	

Attendance sheet internal lab exam

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Vimal Jyothi Engineering College

Department of Electronics Communication and Engineering (EC)

USN	Name	Present (P) / Absent (Ab)	Experiment	IA Total
VML21EC034	K Amith Babu	P	6	28
VML21EC035	Manu Roy	P	1	10
VML21EC036	Martin Reju	P	3	27
VML21EC037	Midhun Madhav M	P	6	18
VML21EC038	Muhammad Saleeth	P	3	22
VML21EC039	Muhammed Aadil Ashraf	P	9	15
VML21EC040	Navya.t	P	8	9
VML21EC041	Neha.m	P	7	14
VML21EC042	Rana Noufal	P	4	25
VML21EC043	Rithwik M R	P	3	21
VML21EC044	Sayand Shine K	P	6	10
VML21EC045	Sebastian Joseph	P	5	15
VML21EC046	Soorya M S	P	3	14
VML21EC047	Sreelal P V	P	5	26
VML21EC048	Theertha Sunil	P	8	9
VML21EC049	Vaishnavi E	P	3	23

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VIMAL JYOTHI ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ECL 204-MICROCONTROLLER LAB

SEMESTER 4 (2021-25 BATCH)

INTERNAL LAB EXAMINATION (26.06.2023 TO 27.06.23)

SLNO	USN / Candidate ID	NAME OF STUDENTS	INTERNAL ASSESSMENT			
			IMPLIMENTATION (10)	RESULT (10)	VIVA (10)	TOTAL (30)
1	VML21EC001	Abhinav Prakash	5	0	7	12
2	VML21EC002	Abhinav Sujith	7	0	4	11
3	VML21EC003	Adarsh K B	10	10	7	27
4	VML21EC004	Aeibel Tomy	10	10	6	26
5	VML21EC005	Ahammed Sinan Muhammed	10	10	8	28
6	VML21EC006	Ajaynath P	7	5	9	21
7	VML21EC007	Akarsh Kc	10	10	7	27
8	VML21EC008	Alanta George	10	10	9	29
9	VML21EC009	Amal Sony	10	10	4	24
10	VML21EC010	Amith Vinesh	0	0	3	3
11	VML21EC011	Amrutha A Nair	10	10	10	30
12	VML21EC012	Ananya K	6	0	6	12
13	VML21EC013	Angel Mary	10	10	9	29
14	VML21EC014	Ann Mariya Chacko	6	0	10	16
15	VML21EC015	Anold Tomy	6	0	8	14
16	VML21EC016	Anukrishna P V	5	0	4	9

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47	VML21EC047	Sreelal P V	10	10	6	26
48	VML21EC048	Theertha Sunil	5	0	4	9
49	VML21EC049	Vaishnavi E	8	10	5	23
50	VML21EC050	Vishakh Sasi	10	10	10	30
51	VML21EC051	Vismaya C	5	0	10	15
52	LVML21EC052	Sidharth C	5	0	4	9
53	LVML21EC053	Vishnupriya M P	7	2	8	17
54	SCT21EC088	Samved Vivek	← Absent →			

Internal Examiner's

Sudharsana Vijayan. 27/6/23.

Anusha Chacko. 27/6/23

Internal Lab Exam mark distribution sheet

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*Generated on: 2023-07-12,09:44:20

APJ Abdul Kalam Technological University
CET Campus, Thiruvananthapuram
Kerala -695016
India

VIMALJYOTHI ENGINEERING COLLEGE

Students Examination Eligibility Details

Academic Year : 2022 - 2023 **Degree Type : Regular**

Program : B.Tech(Full Time) **Branch : ELECTRONICS AND COMMUNICATION ENGINEERING** **Semester : S4**

Course Name : MICROCONTROLLER LAB- ECL204 **Batch : 1**

Eligibility For : Pursuing Students **Period of Registration : NA**

Student Name	Attendance %, Internal Marks/75	Availed Leaves	Disc. Action	Eligible for Written Exam	Status:	In-eligibility Type
ABHINAV PRAKASH Register No : VML21EC001	Attendance : 100.0 Internal Marks : 56.0/75	Long Leave : Duty Leave :		Yes	Submitted by college	
ABHINAV SUJITH Register No : VML21EC002	Attendance : 100.0 Internal Marks : 53.0/75	Long Leave : Duty Leave :		Yes	Submitted by college	
ADARSH K B Register No : VML21EC003	Attendance : 100.0 Internal Marks : 71.0/75	Long Leave : Duty Leave :		Yes	Submitted by college	

Student eligibility report-submitted in ktu portal

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